Description

The HWA1250 is a high-efficiency, wide instantaneous bandwidth, fully input/output matched power amplifier (PA) with high gain and linearity.

The compact 16-pin 5 × 5 mm PA is designed for FDD and TDD systems, supports 4G LTE bands 7, 38, 41 and 69 and 5G NR FR1 bands n7, n38, n41 and n90 Wireless Infrastructure operating from 2500 to 2700MHz.

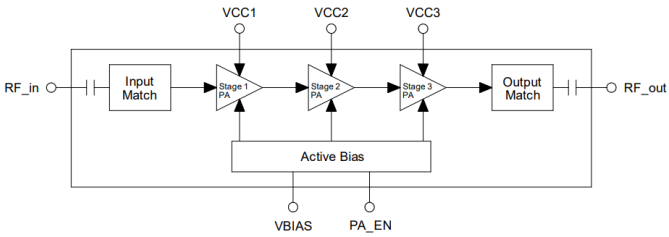
The active biasing circuitry is integrated to compensate PA performance over temperature, voltage, and process variation.

This amplifier is part of Hexawave's high-efficiency 4W PA RF product line designed for wireless infrastructure supporting major 3GPP bands.

Features

- **Wide instantaneous signal bandwidth**：200 MHz
- **High Efficiency**：PAE = 36.4% @ Pout = 28 dBm
- **High Linearity**：ACLR < -50 dBc @ Pout = 28 dBm with DPD (5G NR, 8.5 dB PAR CCDF 0.01% signal)
- **High output power**：Psat > 35 dBm
- **High power gain**：33 dB
- **Single supply voltage**：Vcc = 5.0 V
- **Integrated enable On/Off function**：PAEN = 2.0 V
- **Integrated active bias**：performance compensated over temp
- **50 Ω matched input and output**
- **Compact (16-pin, 5.0 × 5.0 × 1.07 mm) package (MSL3, 260 °C per JEDEC J-STD-020)**

Functional Block Diagram



Applications

- **Supports 5G and 4G FDD and TDD systems**
- **Supports 3GPP 4G LTE bands 7, 38, 41 and 69**
- **Supports 3GPP 5G NR FR1 bands n7, n38, n41 and n90**
- **Small cells for wireless communications infrastructure and massive MIMO**
- **Repeaters / DAS**
- **General purpose wireless**

■Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
RF Input Power (CW)	P_{IN}		+10	dBm
Supply Voltage (VCC1, 2, 3 and VBIAS)	V_{CC}		5.5	V
PA Enable	V_{EN}		3.6	V
Operating Temperature	T_{op}	-40	+110	℃
Storage Temperature	T_{STG}	-55	+125	℃
Junction Temperature (for 10^6 hours MTTF)	T_J		+175	℃
Power Dissipation	P_D		1.1	W
Device Thermal Resistance	θ_{JC}		15	℃/W
Electrostatic Discharge： ***Charged Device Model (CDM)*** ***Human Body Model (HBM)***	ESD		 500 1000	 V V

Note：If the satisfied of any one or more of the above conditions will lead to equipment damage.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

■Recommended Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Operation Frequency	Freq.	2.3		2.7	GHz
Supply Voltage (VCC1, 2, 3 and VBIAS)	V_{CC}	4.75	5.0	5.5	V
PA Enable ***ON*** ***OFF***	V_{EN}	1.7	 2.0 0	 3.6 0.5	V
PA Enable Current*	I_{EN}		5	10	uA
Operation Temperature	T_C	-40	+25	+110	℃

**Note：This current is when PA Enable is 2V, if the voltage increases, the current will also increase accordingly.*

■Electrical Specifications

VCC1, 2, 3 = VBIAS = 5.0V, PA_EN = 2.0V, Freq. = 2600MHz, TC = 25℃, Input/Output Impedance 50Ω, unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Frequency	Freq.		2300		2700	MHz
Small Signal Gain	|S21|	P_{IN} = -30dBm		33		dB
Gain @+28dBm	|S21|	P_{OUT} = +28dBm		33		dB
Input Return Loss	|S11|	P_{IN} = -30dBm		20.7		dB
Output Return Loss	|S22|	P_{IN} = -30dBm		25.6		dB
Reverse Isolation	|S12|	P_{IN} = -30dBm		54		dB
ACLR @+28dBm	ACLR	P_{OUT} = +28dBm (100MHz 5G NR, 8.5dB PAR Signal)		-25.6		dBc
Output Power for 1 dB Compression	OP1dB	CW, Reference to Gain (Pout = 20dBm)		35.8		dBm
Saturated Output Power	P_{SAT}	Use duty cycle100% CW tone		36.2		dBm
2nd Harmonic	$2f_0$	CW, P_{OUT} = +28dBm		-54.5		dBc
3rd Harmonic	$3f_0$	CW, P_{OUT} = +28dBm		-57.3		dBc
Power Added Efficiency	PAE	CW, P_{OUT} = +28dBm		36.4		%
Total Operating Current	I_{total}	Pin 5, 12, 14 and 16 P_{OUT} = +28dBm		340		mA
Quiescent Current	I_{CQ}	No RF Signal		93		mA
RF turn-on / turn-off time				200		ns

Notes：

1. *Performance is guaranteed only under the conditions listed in this table.*
2. *Not tested in production. Verified by design.*
3. *RF turn-on time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power achieves 90% of the average steady-state "on" level.*
4. *RF turn-off time is measured from the time the PA enable reaches 50% of PA enable "on" level to the time at which the RF output power decreases to 10% of the average steady-state "on" level.*

■Typical Performance Characteristics

VCC1, 2, 3 = VBIAS = 5.0V, PA_EN = 2.0V, Freq. = 2600MHz, TC = 25℃, Input/Output Impedance = 50Ω, unless otherwise noted

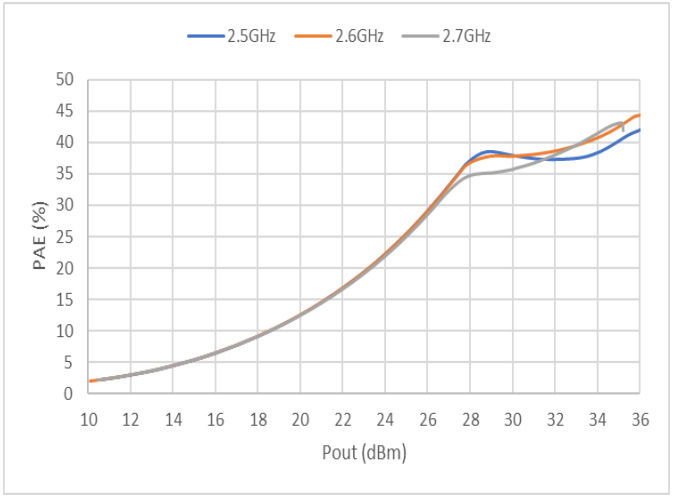


Figure 1. PAE vs Pout (CW) Across Frequency

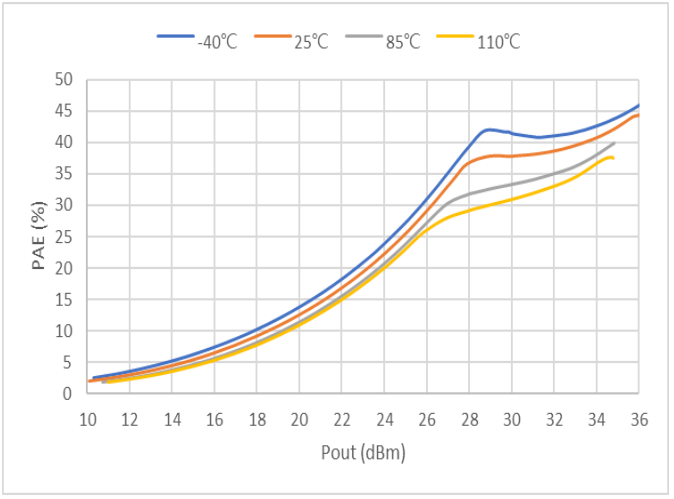


Figure 2. PAE vs Pout (CW) Across Temperature

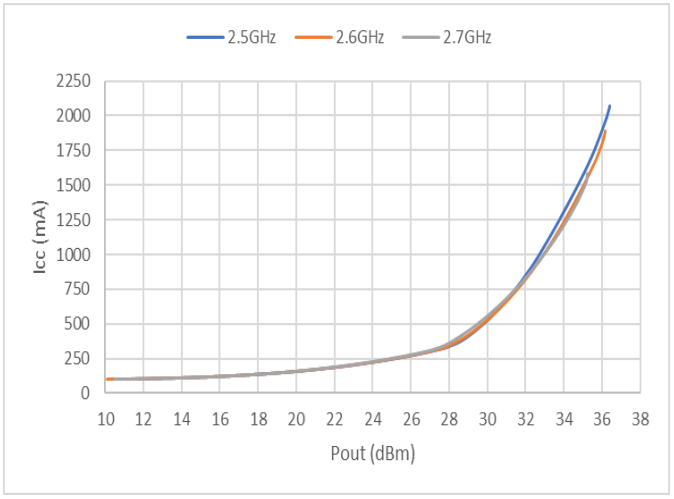


Figure 3. Icc vs Pout Across Frequency

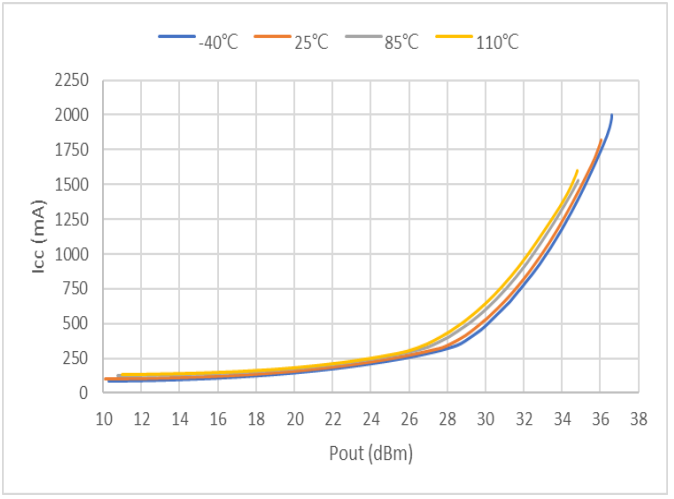


Figure 4. Icc vs Pout Across Temperature

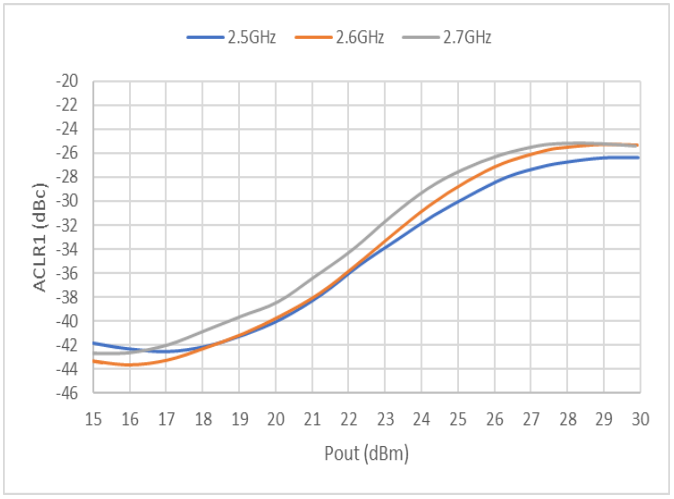


Figure 5. ACLR (1x100 MHz) vs Pout Across Frequency

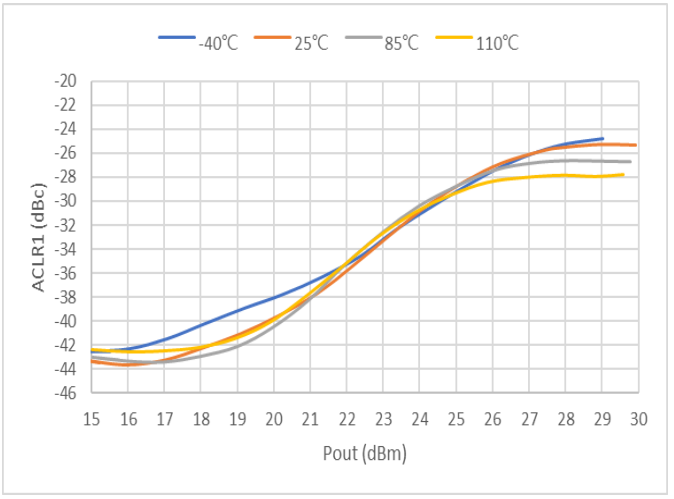


Figure 6. ACLR (1x100 MHz) vs Pout Across Temperature

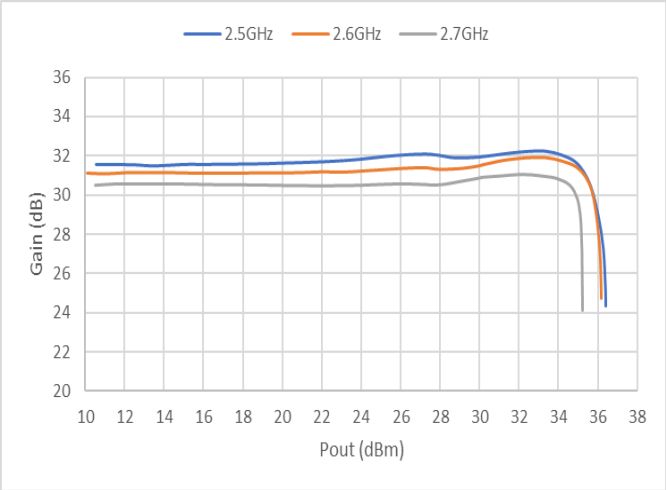


Figure 7. Gain vs Pout Across Frequency

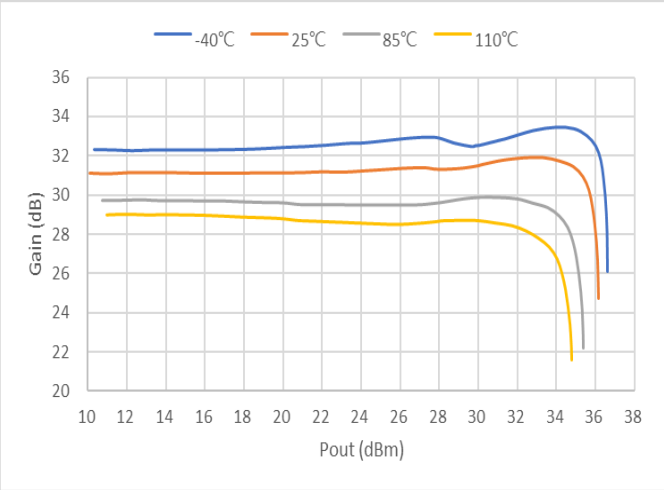


Figure 8. Gain vs Pout Across Temperature

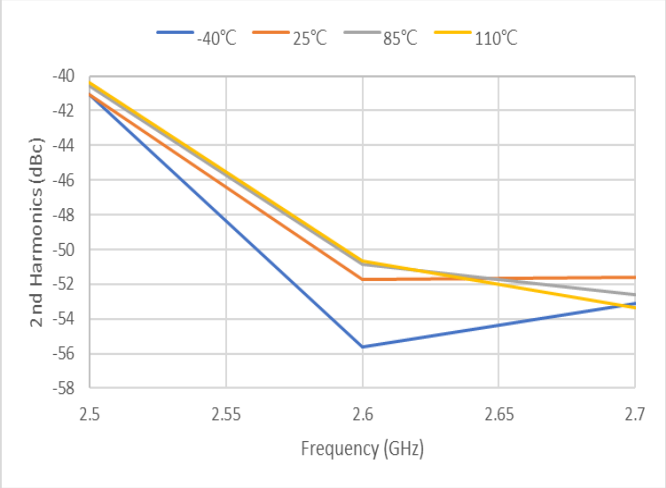


Figure 9. 2nd Harmonic @ +28 dBm (CW) vs Frequency Across Temperature

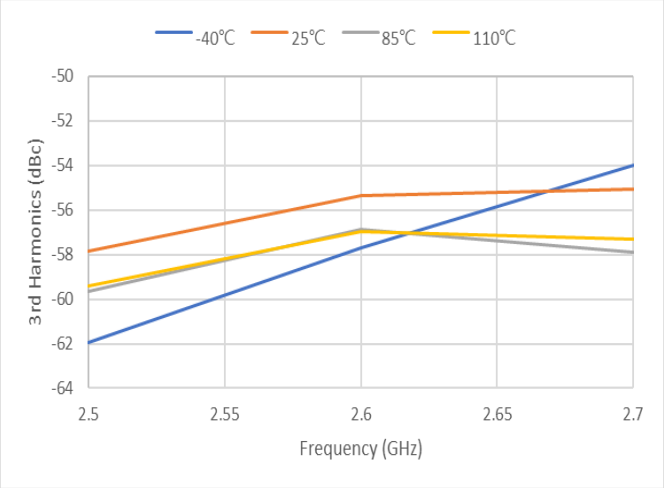


Figure 10. 3rd Harmonic @ +28 dBm (CW) vs Frequency Across Temperature

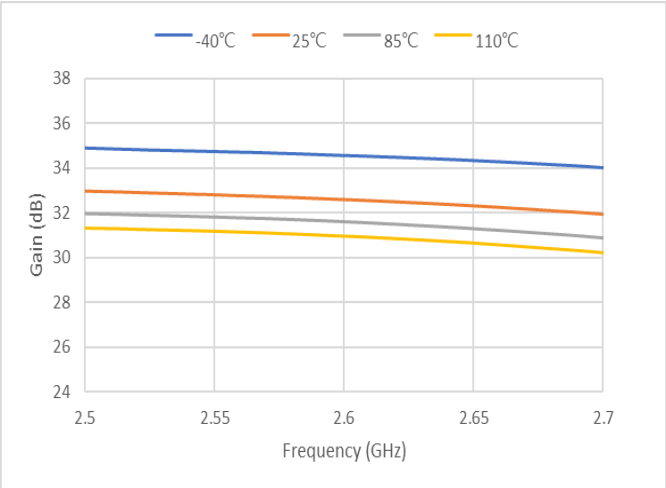


Figure 11. Small Signal Gain vs Frequency Across Temperature

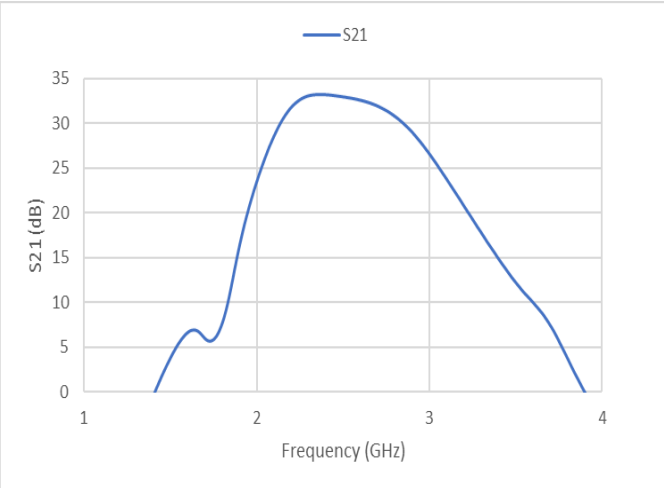


Figure 12. Wide-Band S21 vs Frequency

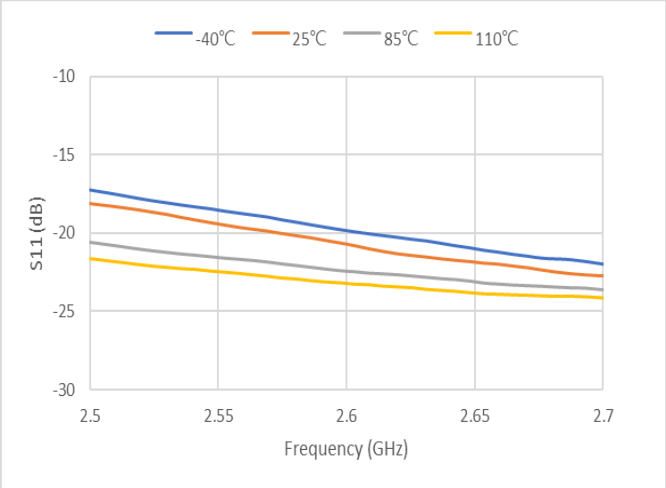


Figure 13. S11 vs Frequency Across Temperature (Pin = -30 dBm)

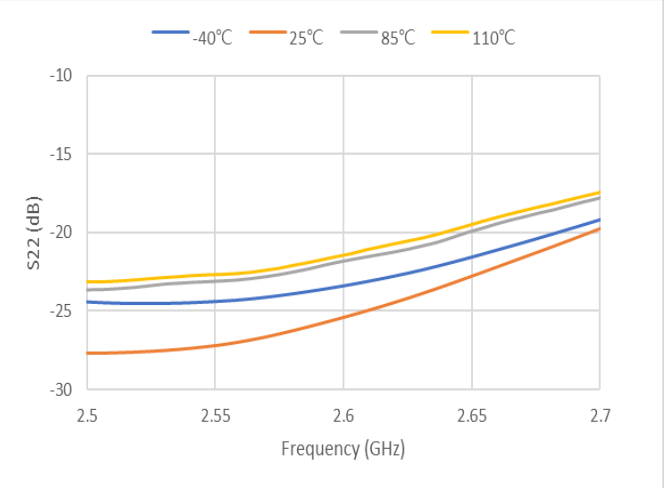
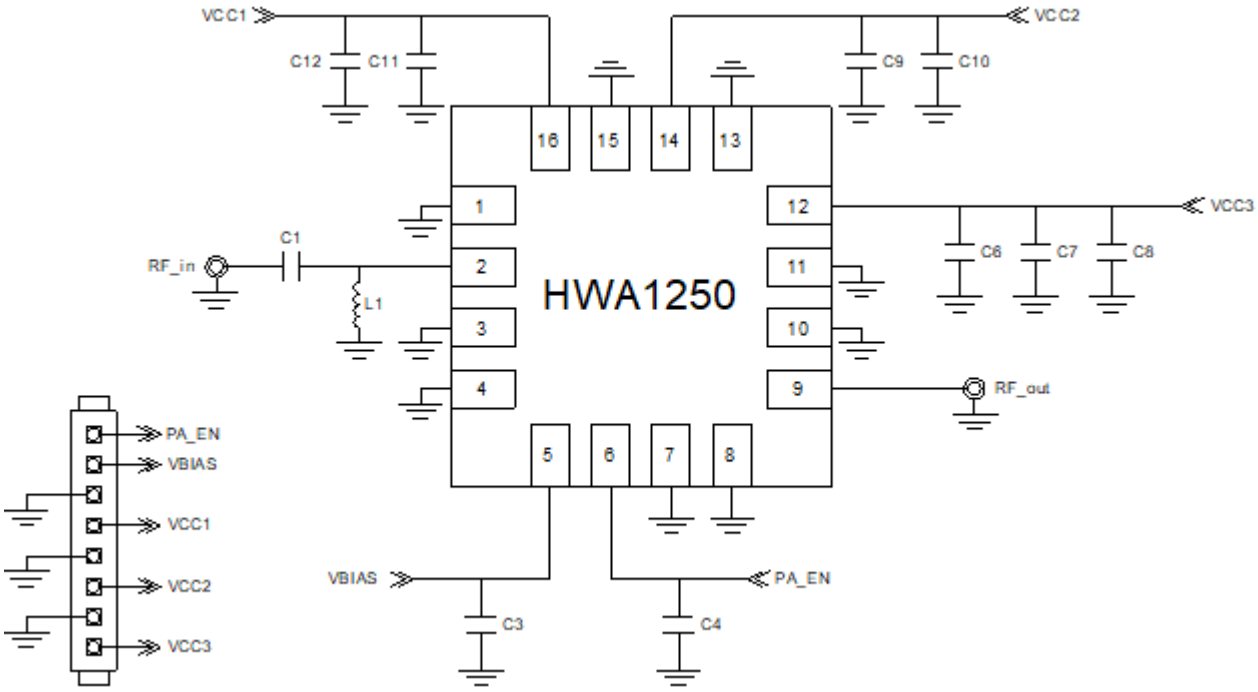


Figure 14. S22 vs Frequency Across Temperature (Pin = -30 dBm)

■Application Circuit



■Pin Assignments

Pin No.	Name	Description	Pin No.	Name	Description
1	GND	Ground	***9***	RF_out	RF Output Port
2	RF_in	RF Input Port	***10***	GND	Ground
3	GND	Ground	***11***	GND	Ground
4	GND	Ground	***12***	VCC3	Stage 3 Collector Voltage
5	VBIAS	Bias Voltage	***13***	GND	Ground
6	PA_EN	PA Enable	***14***	VCC2	Stage 2 Collector Voltage
7	GND	Ground	***15***	GND	Ground
8	GND	Ground	***16***	VCC1	Stage 1 Collector Voltage

Note：

The matching circuits are contained within the device. The HWA1250 is internally matched for maximum output power and efficiency. The input and output stages are independently supplied using the VCC1, VCC2, and VCC3 supply lines (pins 16, 14, and 12, respectively). The DC control voltage that sets the bias is supplied by the VCBIAS signal (pin 5).

■Evaluation Board Bill of Material (BOM)

Component	Value / Part Number	Description
IC	HWA1250	2.3G to 2.7GHz, High-Efficiency Power Amplifier
C1	0R	Resistor, 0402
C3	1uF	Ceramic Capacitor, 0402
C4, C7	3300pF	Ceramic Capacitor, 0402
C6	1uF	Ceramic Capacitor, 0402
C8, C10, C12	10uF	Ceramic Capacitor, 1206
C9	0.47uF	Ceramic Capacitor, 0402
C11	0.1uF	Ceramic Capacitor, 0402
L1	DNI	

Note：The center ground pad must have a low inductance and low thermal resistance connection to the application's printed circuit board ground plane.

■Evaluation Board Test Procedure

✧ Turn-On Sequence

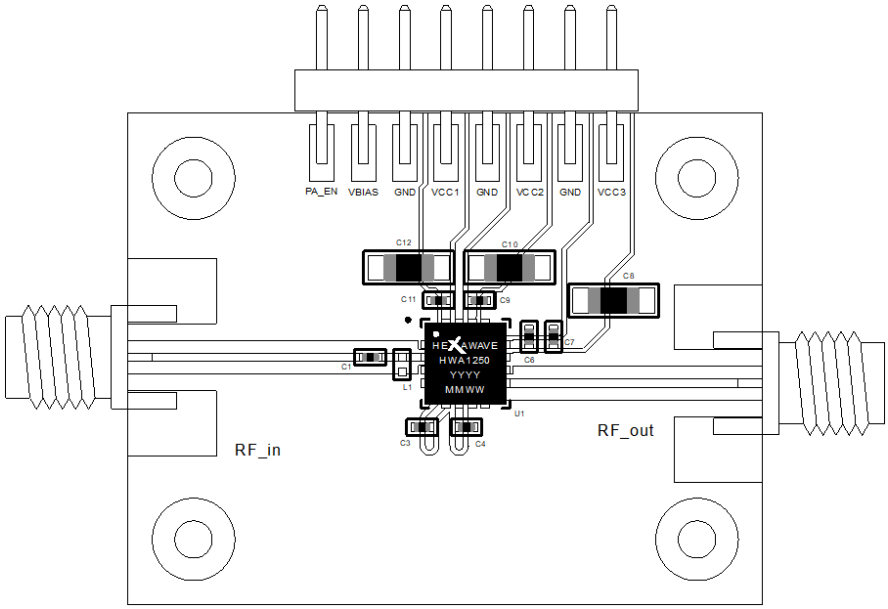
1. Connect 50 Ohm Test Equipment or Load to the input and output RF ports of the Evaluation Board.
2. Connect the DC ground.
3. Connect all VCCs and VBIAS lines to a +5 V supply. Connect PAEN to a 2.0 V supply.
4. Without applying RF, turn on the 5 V supply, then turn on the 2 V PAEN.
5. Apply RF signal data at -30 dBm and observe that the gain of the device is approximately 33 dB. Begin measurements.

✧ Turn-Off Sequence

1. Turn off the RF input to the device.
2. Turn off PAEN (set to 0 V).
3. Turn off all VCCs and VBIAS.

Note：It is important to adjust the VCC voltage sources so that +5 V is measured at the board. High collector currents drop the collector voltage significantly if long leads are used. Adjust the bias voltage to compensate.

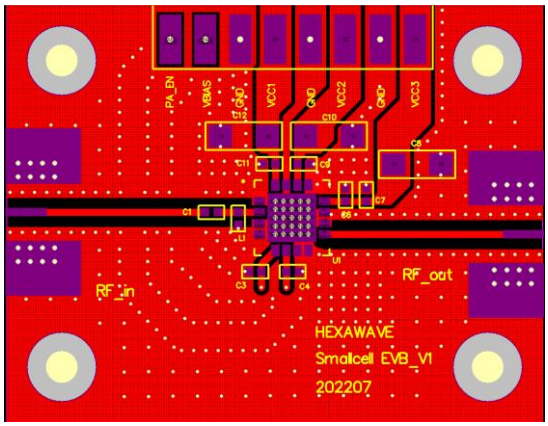
■Evaluation Board Assembly Drawing



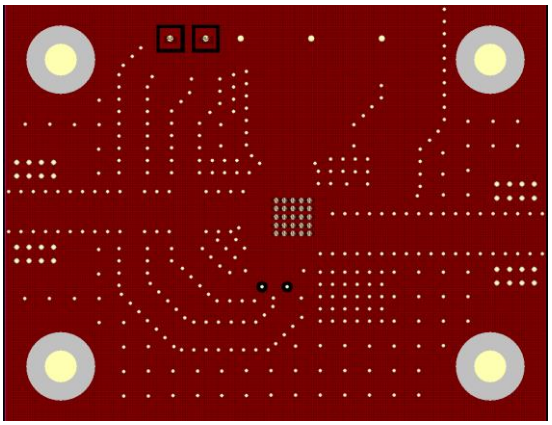
Notes：

1. *The C1 component shown in this assembly is a 0Ωresistor.*
2. *The L1 component shown in this assembly is DNI.*

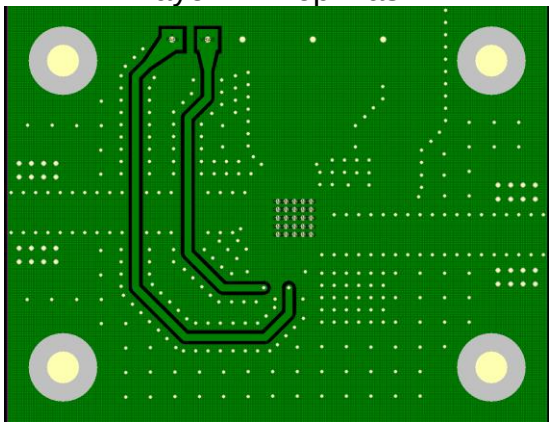
■Board Layer Detail



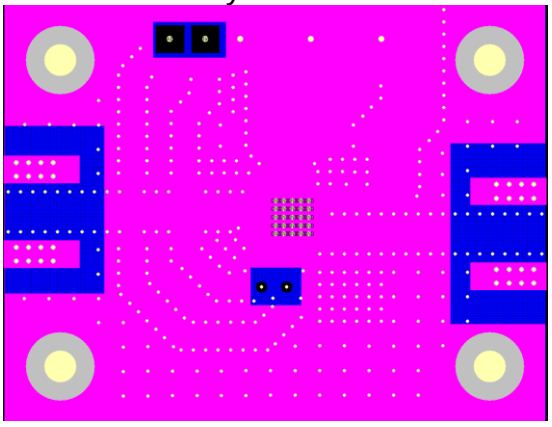
Layer 1 + Top Mask



Layer 2

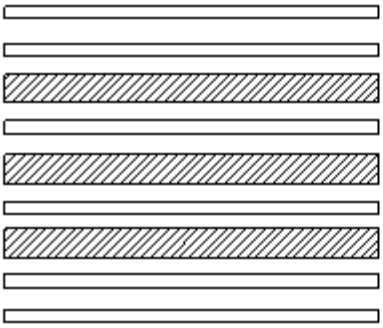


Layer 3



Layer 4 + Bottom Mask

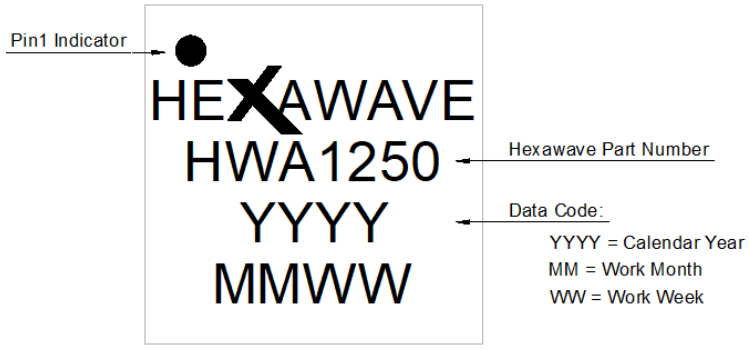
■Layer Detail Physical Characteristics

50 Ohm	Cross Section	Name	Thickness(mm)	Materials
W=0.500mm		TMask	0.010	Solder Resist
		L1	0.035	Cu, 1oz.
		Dielectric	0.250	RO4350
		L2	0.035	Cu, 1oz.
		Dielectric	0.350	FR4
		L3	0.035	Cu, 1oz.
		Dielectric	0.250	FR4
		L4	0.035	Cu, 1oz.
		BMask	0.010	Solder Resist

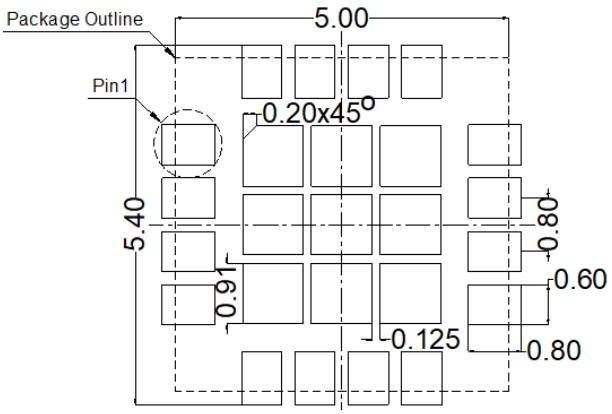
■Application Circuit Notes

1. **Center Ground.** It is extremely important to sufficiently ground the bottom ground pad of the device for both thermal and stability reasons. Multiple small vias are acceptable and work well under the device if solder migration is an issue.
2. **GND (pins 1, 3, 4, 7, 8, 10, 11, 13, and 15).** Attach all ground pins to the RF ground plane with the largest diameter and lowest inductance via that the layout allows. Multiple small vias are acceptable and will work well under the device if solder migration is an issue.
3. **VCBIAS (pin 5).** The bias supply voltage for each stage, nominally set to +5 V.
4. **RFOUT (pin 9).** Amplifier RF output pin (ZO = 50 Ohm). The module includes an internal DC blocking capacitor. All impedance matching is provided internal to the module.
5. **VCC1, VCC2, and VCC3 (pin 16, 15, and 12, respectively).** Supply voltage for each stage collector bias is nominally set to 5 V. The evaluation board has inductors L1 and L2. These are place holders, and should be populated with 0 Ohm resistors. Bypass and decoupling capacitors C6 through C12 should be placed in the approximate location shown on the evaluation board assembly drawing, although exact placement is not critical.
6. **RFIN (pin 2).** Amplifier RF input pin (ZO = 50 ohm). All impedance matching is provided internal to the module.

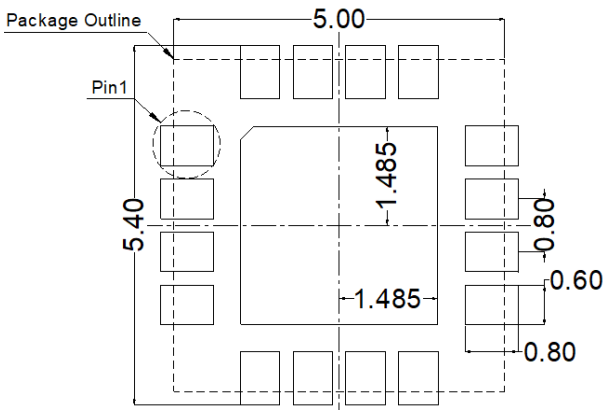
■Typical Part Marking



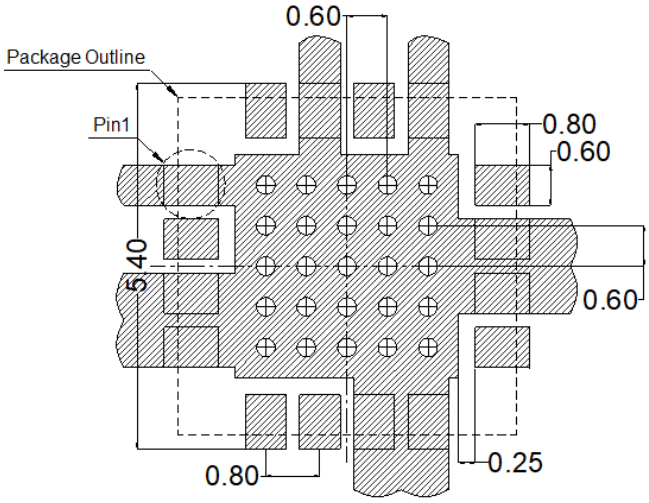
■PCB Layout Footprint Patterns



Stencil Aperture Top View



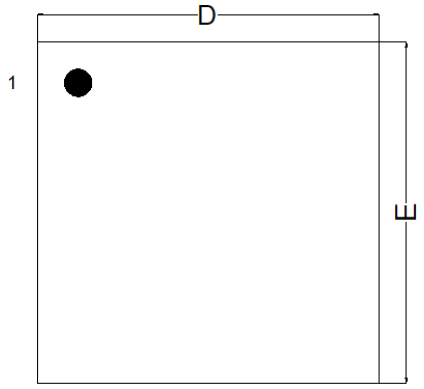
Solder Mask Opening Top View



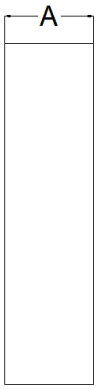
Unit:mm

Metallization Top View

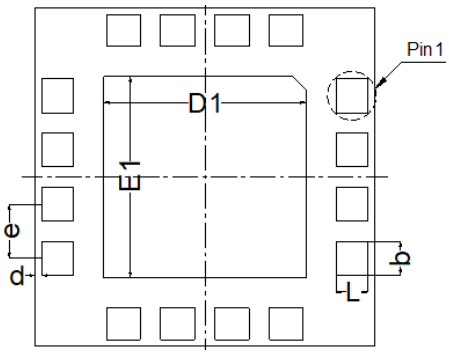
■Package Dimensions



Top View



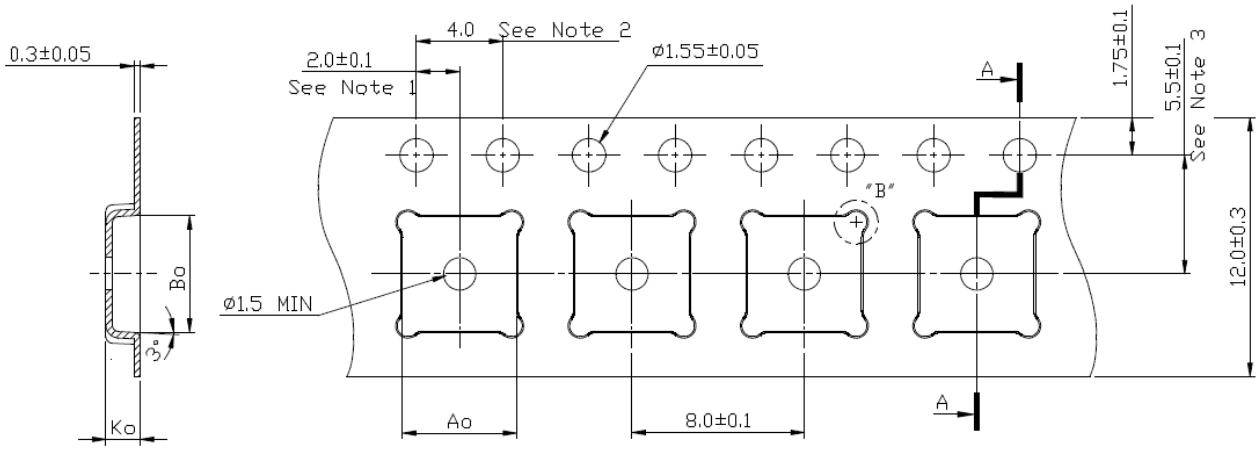
Side View



Bottom View

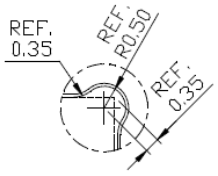
Symbol	Min	Max	Unit
A	1.00	1.14	mm
b	0.45	0.55	
D	4.90	5.10	
D1	2.92	3.02	
d	0.00	0.20	
E	4.90	5.10	
E1	2.92	3.02	
e	0.80 BSC		
L	0.42	0.52	

■HWA1250 Tape and Reel Dimensions



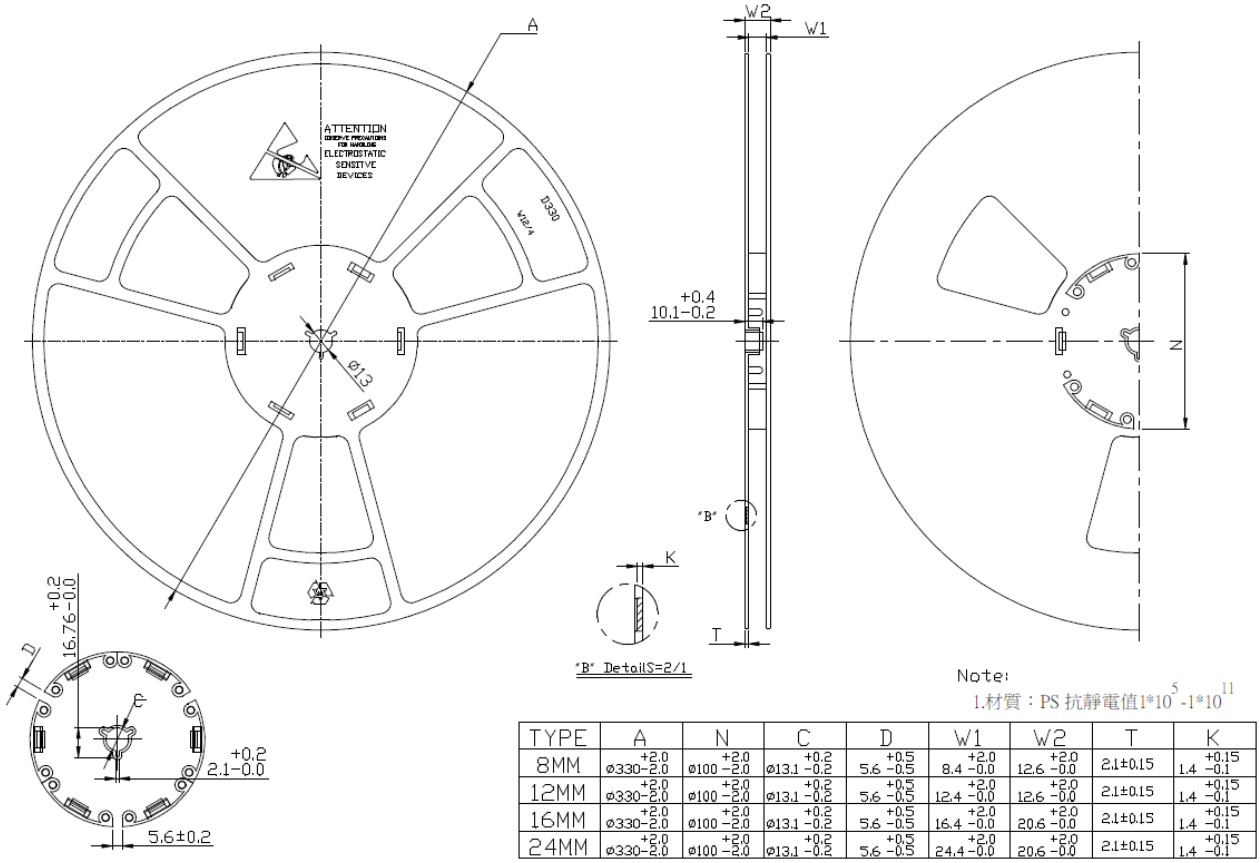
Section A-A

Ao=5.3±0.1mm
Bo=5.3±0.1mm
Ko=1.3±0.1mm



"B" Detail
S=2/1

Notes:
1.Measured from centreline of sprocket hole to centreline of pocket.
2.Cumulative tolerance of 10 sprocket holes is ±0.20.
3.Measured from centreline of sprocket hole to centreline of pocket.
4.Other material available.



"B" Detail S=2/1

Note:
1.材質：PS 抗靜電值$1*10^{5}$ -$1*10^{11}$

TYPE	A	N	C	D	W1	W2	T	K
8MM	ø330 +2.0 −2.0	ø100 +2.0 −2.0	ø13.1 +0.2 −0.2	5.6 +0.5 −0.5	8.4 +2.0 −0.0	12.6 +2.0 −0.0	2.1±0.15	1.4 +0.15 −0.1
12MM	ø330 +2.0 −2.0	ø100 +2.0 −2.0	ø13.1 +0.2 −0.2	5.6 +0.5 −0.5	12.4 +2.0 −0.0	12.6 +2.0 −0.0	2.1±0.15	1.4 +0.15 −0.1
16MM	ø330 +2.0 −2.0	ø100 +2.0 −2.0	ø13.1 +0.2 −0.2	5.6 +0.5 −0.5	16.4 +2.0 −0.0	20.6 +2.0 −0.0	2.1±0.15	1.4 +0.15 −0.1
24MM	ø330 +2.0 −2.0	ø100 +2.0 −2.0	ø13.1 +0.2 −0.2	5.6 +0.5 −0.5	24.4 +2.0 −0.0	20.6 +2.0 −0.0	2.1±0.15	1.4 +0.15 −0.1

■Ordering Information

Part Number	Product Description	Evaluation Board Part Number
HWA1250	2300 to 2700 MHz Wide Instantaneous High-Efficiency PA	HWA1250-EVB